UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,279	07/08/2003	Jack R. Smith	BUR920030010USA	1278

28211 7590 08/24/2005

FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,279	SMITH ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/08/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-33* is/are allowed.

6)☒ Claim(s) *1-13 and 34-40* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 07/08/2003. Claims ~~1-23 and 34-40~~ 1-40 VS. are pending.

Drawings

1. The drawings are objected to because **Figures 1-2** do not comply with 37 CFR 1.84(l). and 37 CFR 1.84(m). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> *(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

3. **Claims 1-13, 15-23, and 34-40** are rejected under 35 U.S.C. 102(b) as being unpatentable by **Segal (US Patent No. 6023568).**

Referring to claim 1, Segal discloses the method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches (*Abstract; Fig. 1; Fig.2-4; col. 1, lines 17-20*); and

creating a physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design (*Abstract; Fig. 1; Fig.2-4*),

wherein said creating of said physical design further comprises eliminating redundant latches , wherein redundant latches comprise latches which do not transition during the same clock cycle (*Fig. 2-4; col. 2, lines 27-39; col. 12, lines 50-53*), do not relate to the same logical function (*Fig. 2-4; col. 2, lines 1-13*), are in the same clock domain (*col.2 , lines 27-39; col. 3, lines 57-61; col. 12, lines 50-53*), and are within a given physical proximity of each other (*Fig. 2-4; col. 2, lines 1-13*).

Referring to claim 2, Segal discloses the method in claim 1, further comprising determining whether latches transition during the same clock cycle by running a simulation of an initial physical design (*Fig. 1; col. 1, lines 14-20*) and recording the latches that transition during each clock cycle (*col. 11, lines 58-64; col. 12, lines 27-31*).

Referring to claim 3, Segal discloses the method in claim 2, wherein said process of determining whether latches transition during the same clock cycle further comprises determining whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle (*col. 2, lines 59+; col. 3, lines 1-8*).

Referring to claim 4. Segal discloses the method in claim 1, wherein said process of eliminating redundant latches comprises replacing at least two redundant latches with a single latch (*Fig.2-4; col. 2, lines 27-39; col. 12, lines 50-53*).

Referring to claim 5, Segal discloses the method in claim 1, wherein said process of eliminating redundant latches produces a revised physical design (*Fig. 3- 4*), and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected (*Abstract; col. 1, lines 13-20*).

Referring to claim 6, Segal discloses the method in claim 1, further comprising determining whether said latches relate to the same logical function by recording which latches are associated with each logical function in said logical design (*col. 8, lines 18-29*).

Referring to claim 7. Segal discloses the method in claim 1, further comprising determining whether said latches are in the same clock domain by recording which latches are associated with each clock domain in said logical design (*Table 1; col. 8, lines 51+*).

Referring to claim 8, Segal discloses the method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches (*Abstract; Fig. 1; Fig.2-4; col. 1, lines 17-20*);

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design (*Abstract; Fig. 1; Fig.2-4*),

preparing a database of transition times *(col. 12, lines 6-8, " the clocks table"*) for said latches by running a simulation of an initial physical design and recording the clock cycle in which each latch transitions (*col. 11, lines 47+; col. 12, lines 1-12*);

altering said initial physical design (*Fig. 2-4; col. 1, lines 17-18*) to eliminate redundant latches which do not transition during the same clock cycle (*Fig. 2-4; col.2 , lines 27-39*).

Referring to claim 9, Segal discloses the method in claim 8, wherein said altering of said initial physical design further considers whether latches relate to the same logical function (Fig. *5; col. 3, lines 57-58*), whether latches are in the same clock domain (*col.2, lines 27-39; col. 3, lines 57-61; col. 12, lines 50-53*), and whether latches are within a given physical proximity of each other (*Fig. 2-4; col. 2, lines 1-13*).

Referring to claim 10, Segal discloses the method in claim 8, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle (*col. 2, lines 59+; col. 3, lines 1-8*).

Referring to claim 11, Segal discloses the method in claim 8, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at least two redundant latches with a single latch (*Fig.2-4; col. 2, lines 27-39; col. 12, lines 50-53*).

Referring to claim 12, Segal discloses the method in claim 8, wherein said altering of said initial physical design to eliminate redundant latches produces a revised physical design (*Fig. 3-4*), and said process further comprises testing said revised physical design to determine

whether said revised physical design performs as expected (*Abstract; col. 1, lines 13-20; col. 10, lines 50+; col. 11, lines 1-25).*

Referring to claim 13, Segal discloses the method in claim 8, further comprising determining whether said latches relate to the same logical function (*Fig. 5; col. 3, lines 57-58*) by recording, in said database, which latches are associated with each logical function in said logical design (*col. 8, lines 18-29*).

Referring to claim 15, Segal discloses the method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches (*Abstract; Fig. 1; Fig.2-4; col. 1, lines 17-20*);

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design (*Abstract; Fig. 1; Fig.2-4*);

preparing a database of transition times (*col. 12, lines 6-8, " the clocks table"*) for said latches by running a simulation of an initial physical design and recording the clock cycle in which each latch transitions (*col. 11, lines 47+; col. 12, lines 1-12*);

altering said initial physical design (Fig. 2-4; *col. 1, lines 17-18*) to eliminate redundant latches which do not transition during the same clock cycle (*Fig. 2-4; col. 2, lines 27-39; col. 12, lines 50-53*), do not relate to the same logical function (Fig. 2-4; col. 2, lines 1-13), are in the same clock domain (*col.2 , lines 27-39; col. 3, lines 57-61; col. 12, lines 50-53*), and are within a given physical proximity of each other (*Fig. 2-4; col. 2, lines 1-13).*

Referring to claim 16, Segal discloses the method in claim 15, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle (*col. 2, lines 59+; col. 3, lines 1-8*).

Referring to claim 17, Segal discloses the method in claim 15, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at least two redundant latches with a single latch (*Fig.2-4; col. 2, lines 27-39; col. 12, lines 50-53*).

Referring to claim 18, Segal discloses the method in claim 15, wherein said altering of said initial physical design to eliminate redundant latches produces a revised physical design

(Fig. 3-4), and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected (*Abstract; col. 1, lines 13-20*).

Referring to claim 19, Segal discloses the method in claim 15, further comprising determining whether said latches relate to the same logical function by recording, in said database, which latches are associated with each logical function in said logical design (*col. 8, lines 18-29*).

Referring to claim 20, Segal discloses the method in claim 15, further comprising determining whether said latches are in the same clock domain by recording, in said database, which latches are associated with each clock domain in said logical design (*Fig. 6; col. 9, lines 4-6; col. 12, lines 27-31*).

Referring to claim 21, Segal discloses the method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches (*Abstract; Fig. 1; Fig.2-4; col. 1, lines 17-20*);

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design (*Abstract; Fig. 1; Fig.2-4*);

preparing a database of transition times for said latches by running a simulation of an initial physical design and recording the clock cycle in which each latch transitions (*col. 12, lines 7-8, " the clocks table"; col. 11, lines 58-64*); determining whether said latches are in the same clock domain by recording, in said database, which latches are associated with each clock domain in said logical design (*Fig. 6; col. 9, lines 4-6; col. 12. , lines 27-31, " hash table");* altering said initial physical design to eliminate redundant latches which do not transition during the same clock cycle (*Fig. 2-4; col.2 , lines 27-39*) , do not relate to the same logical function (*Fig. 2-4; col. 2, lines 1-13*), are in the same clock domain (*col.2 , lines 27-39; col. 3, lines 57-61; col. 12, lines 50-53*), and are within a given physical proximity of each other (*Fig. 2-4; col. 2, lines 1-13)*, wherein said process of altering said initial physical design to eliminate redundant latches produces a revised physical design (*Fig. 3-4*), and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected (Abstract; *col. 1, lines 13-20; col. 10, lines 50+; col. 11, lines 1-25).*

Referring to claim 22, Segal discloses the method in claim 21, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle (*col. 2, lines 59+; col. 3, lines 1-8*).

Referring to claim 23, Segal discloses the method in claim 21, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at least two redundant latches with a single latch (*Fig.2-4; col. 2, lines 27-39; col. 12, lines 50-53*).

Referring to claim 34, Segal discloses the program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of designing an integrated circuit having latches, said method comprising:

preparing a logical design of logic devices and latches (*Abstract; Fig. 1; Fig.2-4; col. 1, lines 17-20*);

creating an initial physical design by positioning said logic devices and said latches within said integrated circuit based on said logical design (*Abstract; Fig. 1; Fig.2-4*);

preparing a database of transition times for said latches by running a simulation of an initial physical design (*Fig. 1; col. 1, lines 14-20*) and recording the clock cycle in which each latch transitions (*col. 2, lines 59+; col. 3, lines1-8*);

altering said initial physical design to eliminate redundant latches which do not transition during the same clock cycle (*Fig. 2-4; col. 2, lines 27-39*).

Referring to claim 35, Segal discloses the program storage device in claim 34, wherein said altering of said initial physical design further considers whether latches relate to the same logical function (*Fig. 5; col. 3, lines 57-58*), whether latches are in the same clock domain (*col. 2, lines 30-34; col. 3, lines 58-61*), and whether latches are within a given physical proximity of each other (*Fig. 2-4; col. 2, lines 1-13*).

Referring to claim 36, Segal discloses the program storage device in claim 34, wherein said altering of said initial physical design further considers whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle (*col. 2, lines 59+;col. 3, lines 1-8*).

Referring to claim 37, Segal discloses the program storage device in claim 34, wherein said altering of said initial physical design to eliminate redundant latches comprises replacing at

least two redundant latches with a single latch (*Fig.2-4; col. 2, lines 27-39*).

Referring to claim 38, Segal discloses the program storage device in claim 34, wherein said altering of said initial physical design to eliminate redundant latches produces a revised physical design (Fig. 3-4), and said process further comprises testing said revised physical design to determine whether said revised physical design performs as expected (Abstract; *col. 1, lines 13-20; col. 10, lines 50+; col. 11, lines 1-25*).

Referring to claim 39, Segal discloses the program storage device in claim 34, wherein said method further comprises determining whether said latches relate to the same logical function by recording, in said database, which latches are associated with each logical function in said logical design (*col. 8, lines 18-29*).

Referring claim 40, Segal discloses the program storage device in claim 34, wherein said method further comprises determining whether said latches are in the same clock domain by recording, in said database, which latches are associated with each clock domain in said logical design (Fig. *6; col. 9, lines 4-6*).

Allowable Subject Matter

4. **Claim 14** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 24-33 are allowed.

Claim 14 would be allowable and claims 24-33 are allowed because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 14)

wherein said selection logic locks a non-active output to a known logical state when another output is active.

(Claims 24-33)

adding selection logic connected to said latches in said revised physical design , wherein said selection logic includes outputs equal in number to the number of latches in said initial physical design and said selection logic locks a non-active output to a known logical state when a corresponding output is active .

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-293-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
Patent Examiner

VUTHE SIEK
PRIMARY EXAMINER